TECHNICAL DATA

LeCroy

CAMAC Model 2228
Octal Time-to-Digital Converter

* **8 channels in single-width module**
* **10-bit (1024 channel) resolution**
* **Switch-selectable 102 ns, 204 ns, and 510 ns full-scale time ranges.**
* **Time resolutions of 100 ps, 200 ps, or 500 ps**
* **Rejects stops before starts**
* **Fast clear input**
* **Internal test capability**
* **Common stop input for precision on-line testing**
* **Full LAM functions**
* **Fast digitizing time**
* **Q and LAM suppression**

The LRS Model 2228 Octal Time-to-Digital Converter, the state-of-the-art successor to the popular Model 2226A Quad TDC, incorporates all the advanced operating characteristics which experience has indicated necessary for accurate and reliable measurement of nanosecond time intervals.

The Model 2228 has 8 independent channels, each of which measures the time from the leading edge of a common start pulse to the leading edge of its individual stop pulse. Each 2228 channel disregards any stop pulses received before a start signal and will accept only one stop for every start.

Conversion begins upon receipt of the start signal and proceeds until one of the following: a stop signal is received; the cycle is terminated by the application of a front-panel clear signal; or the TDC reaches full scale.

The 2228 converts the measured time intervals into a 10-bit digital number at the rate of 20 MHz, for a full scale digitizing time of 50 microseconds. The conversion clock is started in phase with the TDC start signal to assure synchronization and eliminate the inaccuracy introduced by the free-running oscillators in conventional designs. LAM, if enabled, is generated at the end of the conversion interval.

The 2228 has three switch-selectable full-scale time ranges, 102 ns, 204 ns, and 510 ns, which are digitized to 10 bits (1024 channels) and provide 100 ps, 200 ps, and 500 ps resolutions respectively. Longer time ranges (up to a few microseconds) may be provided on request at slight expense of stability and accuracy.

On-line testing is facilitated by either a front-panel common stop input or F(25). A signal at the common stop input generates simultaneous stops for each channel, permitting accurate testing of both front end and scaler section of the module and uniform system testing and calibration. F(25) is provided for a quick test of the front end and scaler sections with a time measurement of ≈75 ns.

In high rate experiments, excessive system deadtime due to false starts may be eliminated through use of the 2228's fast clear input. Accepting NIM level signals, this input allows the TDC to be cleared within 2 microseconds at any point in its conversion cycle and without the necessity for any dataway operations.

All standard LAM functions are available in the 2228 to facilitate data readout. To minimize readout time, both Q and LAM may be suppressed if the module does not contain data.

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SPECIFICATIONS
CAMAC Model 2228
OCTAL TIME-TO-DIGITAL CONVERTER

Stop Inputs:	8, one per channel; 50 Ω impedance; Lemo-type connectors; direct-coupled; input amplitude > —600 mV; ineffective unless preceded by a "Start" input.
Common Start Input:	One, common to all channels; 50 Ω impedance; Lemo-type connector; input amplitude > −600 mV.
Common Stop Input:	One, common to all channels; 50 Ω impedance; Lemo-type connector; > −600 mV; functions identical to individual "Stop Inputs" above; used for precision on-line testing.
Fast Clear:	One input common to all channels; Lemo-type connector; 50 Ω impedance; −600 mV or greater clears; minimum duration, 50 ns. (Caution: narrower pulses cause partial clearing.) Requires additional 2.0 μs settling time after clear.
Full-Scale Time Range:	10-bit binary output corresponds to 102 ns, 204 ns, and 510 ns, switch selectable (with longest range field adjustable up to 1 μsec). Larger full-scales possible by factory option at slight expense of accuracy and stability, giving 1 μsec, 2 μsec, and 5 μsec as the 3 switch-selectable time ranges.
Integral Non-linearity:	± 2 counts (10 ns to full scale). Set of linearity curves for all channels supplied with each unit. (See graph below.)
Time Resolution:	100 ps on 102 ns range; 200 ps on 204 ns range; 500 ps on 510 ns range.
Temperature Coefficient:	Typically (+ 0.02% of full scale ± 0.01% of reading) per degree C.
Digitizing Time:	60 μsec; conversion is initiated by receipt of "Start" input.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Test Functions:	An internal start/stop is generated by F(25) with ≈75 ns spacing. Precision on-line testing and calibrating can be done with common start and common stop above.
Data:	The proper CAMAC function and address command gates the 10 binary bits plus overflow bit of the selected channel onto the R(1) to R(11) (2^0 to 2^{10}) Dataway bus lines.
CAMAC Commands:	Z or C: All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S2." I: "Start" input is inhibited during CAMAC "Inhibit" command. Q: A Q=1 response is generated in recognition of an F0 or F2 Read function, or an F8 function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules is suppressed (see Q and LAM suppression). X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from end of digitizing until a module Clear or Clear LAM. LAM is disabled for duration of N, can be permanently enabled or disabled by the Enable or Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed by empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A. A(0) through A(7) are used for channel address. F(2): Read registers and clear module; requires N, A, and S2. Clears on A(7) only. F(8): Test Look-At-Me; requires LAM, N, and any A from A(0) to A(7) independent of Disable Look-At-Me. Q is generated if LAM is present. F(9): Clear module (and LAM); requires N and A, and S2. F(10): Clear Look-At-Me; requires N, S2, and any A from A(0) to A(7). F(24): Disable Look-At-Me; requires N, S2 and any A from A(0) to A(7). F(25): Test module; requires N, S2, and any A from A(0) to A(7). F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(7). Remains enabled until Z or F(24) applied. Caution: The state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	A module receiving no stop inputs will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging:	In conformance with CAMAC standard for nuclear modules. RF-shielded CAMAC #1 module.
Power Requirements:	+24 V at 20 mA; —24 V at 50 mA; +6 V at 550 mA; —6 V at 550 mA.

TYPICAL 2228 INTEGRAL LINEARITY